

General Description

The MAX705-MAX708/MAX813L microprocessor (μ P) supervisory circuits reduce the complexity and number of components required to monitor power-supply and battery functions in μ P systems. These devices significantly improve system reliability and accuracy compared to separate ICs or discrete components.

The MAX705/MAX706/MAX813L provide four functions:

- 1) A reset output during power-up, power-down, and brownout conditions.
- 2) An independent watchdog output that goes low if the watchdog input has not been toggled within 1.6 seconds.
- 3) A 1.25V threshold detector for power-fail warning, low-battery detection, or for monitoring a power supply other than +5V.
- 4) An active-low manual-reset input.

The MAX707/MAX708 are the same as the MAX705/MAX706, except an active-high reset is substituted for the watchdog timer. The MAX813L is the same as the MAX705, except RESET is provided instead of RESET.

Two supply-voltage monitor levels are available: The MAX705/MAX707/MAX813L generate a reset pulse when the supply voltage drops below 4.65V, while the MAX706/MAX708 generate a reset pulse below 4.40V. All four parts are available in 8-pin DIP, SO and μ MAX packages.

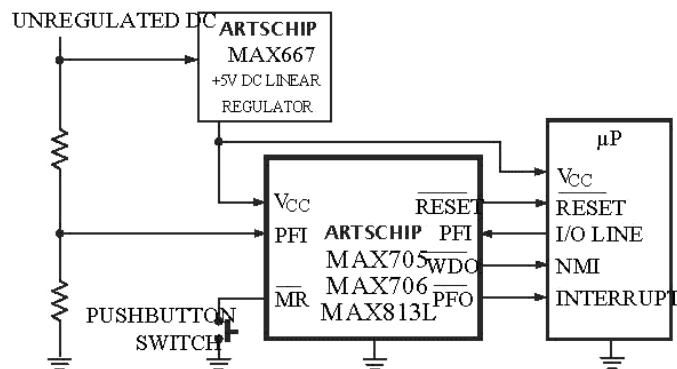
Applications

- Computers
- Controllers
- Intelligent Instruments
- Automotive Systems
- Critical μ P Power Monitoring

Features

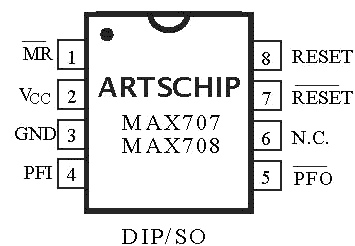
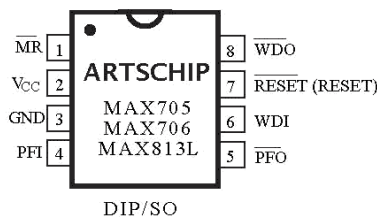
- μ MAX Package: Smallest 8-Pin SO
- Guaranteed RESET Valid at $V_{CC}=1V$
- Precision Supply-Voltage Monitor
 - 4.65V in MAX705/MAX707/MAX813L
 - 4.40V in MAX706/MAX708
- 200ms Reset Pulse Width
- Debounced TTL/CMOS-Compatible Manual-Reset Input
- Independent Watchdog Timer – 1.6sec Timeout (MAX705/MAX706)
- Active-high Reset Output (MAX707/MAX708/MAX813L)
- Voltage Monitor for Power-Fail or Low-Battery Warning

Typical Operating Circuit



Pin Configurations

TOP VIEW



()ARE FOR MAX813L ONLY.

Pin Configurations continued at end of data sheet.



Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX705CPA	0 to +70	8 Plastic DIP
MAX705CSA	0 to +70	8 SO
MAX705CUA	0 to +70	8 μ MAX
MAX705C/D	0 to +70	Dice*

Ordering Information continued at end of data sheet.

*Dice are specified at $T_A=+25$.

**Contact factory for availability and processing to MIL-STD-883.

ABSOLUTE MAXIMUM RATINGS

Terminal Voltage (with respect to GND)
 Vcc.....-0.3V to 6.0V
 All Other Inputs (Note 1).....-0.3V to (Vcc+0.3V)
 Input Current
 Vcc.....20mA
 GND.....20mA
 Output Current (all outputs).....20mA
 Continuous Power Dissipation
 Plastic DIP (derate 9.09 mW/ above +70)...727mW

SO (derate 5.88mW/ above +70).....471mW
 μ MAX (derate 4.10mW/ above +70).....330mW
 CERDIP (derate 8.00mW/ above +70).....640mW

Operating Temperature Ranges

MAX70_C_, MAX813LC_.....0 to +70
 MAX70_E_, MAX813LE_.....-40 to +85
 MAX70_MJA.....-55 to +125
 Storage Temperature Range.....-65 to +160
 Lead Temperature (soldering, 10sec).....+300

Note 1: The input voltage limits on PFI and MR can be exceeded if the input current is less than 10mA.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

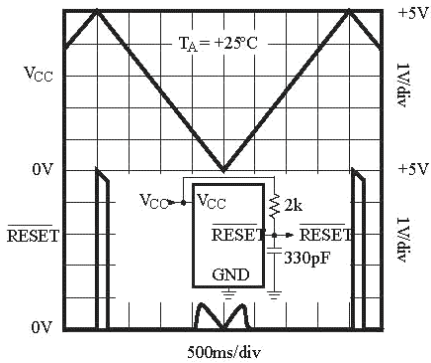
(V_{CC}=4.75V to 5.5V for MAX705/MAX707/MAX813L, V_{CC}=4.5V to 5.5V for MAX706/MAX708, T_A=T_{MIN} to T_{MAX} unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
Operating Voltage Range	V _{CC}	MAX70_C	1.0		5.5	V	
		MAX813LC	1.1		5.5		
		MAX70_E/M,MAX813LE/M	1.2		5.5		
Supply Current	I _{SUPPLY}	MAX705C,MAX706C,MAX813LC		150	350	μ A	
		MAX705E/M,MAX706E/M,MAX813LE/M		150	500		
		MAX707C,MAX708C		50	350		
		MAX707E/M,MAX708E/M		50	500		
Reset Threshold (Note 2)	V _{RT}	MAX705,MAX707,MAX813L	4.50	4.65	4.75	V	
		MAX706,MAX708	4.25	4.40	4.50		
Reset Threshold Hysteresis (Note2)				40		mV	
Reset Pulse Width (Note 2)	t _{RS}		140	200	280	ms	
RESET Output Voltage		I _{SOURCE} =800 μ A	V _{CC} -1.5			V	
		I _{SINK} =3.2mA			0.4		
		MAX70_C, V _{CC} =1V, I _{SINK} =50 μ A			0.3		
		MAX70_E/M, V _{CC} =1.2V, I _{SINK} =100 μ A			0.3		
RESET Output Voltage		MAX707, MAX708,I _{SOURCE} =800 μ A	V _{CC} -1.5			V	
		MAX707,MAX708,I _{SINK} =1.2mA			0.4		
		MAX813LC, I _{SOURCE} =4 μ A, V _{CC} =1.1V	0.8				
		MAX813LE/M, I _{SOURCE} =4 μ A, V _{CC} =1.2V	0.9				
		MAX813L	I _{SOURCE} =800 μ A	V _{CC} -1.5			
			I _{SINK} =3.2mA				0.4
Watchdog Timeout Period	t _{WD}	MAX705, MAX706,MAX813L	1.00	1.60	2.25	sec	
WDI Pulse Width	t _{WP}	V _{IL} =0.4V, V _{IH} – (V _{CC})(0.8)	50			ns	
WDI Input Threshold	Low	MAX705, MAX706, MAX813L, V _{CC} =5V	3.5		0.8	V	
	High						
WDI Input Current		MAX705, MAX706,MAX813L ,WDI=V _{CC}		50	150	μ A	
		MAX705, MAX706,MAX813L,WDI=0V	-150	-50			
WDO Output Voltage		MAX705,MAX706,MAX813L, I _{SOURCE} =800 μ A	V _{CC} -1.5			V	
		MAX705,MAX706,MAX813L, I _{SINK} =1.2mA			0.4		
MR Pull-Up Current		MR=0V	100	250	600	μ A	
MR Pulse Width	t _{MR}		150			ns	
MR Input Threshold	Low		2.0		0.8	V	
	High						
MR to Reset Out Delay (Note 2)	t _{MD}				250	ns	
PFI Input Threshold		V _{CC} =5V	1.20	1.25	1.30	V	
PFI Input Current			-25.00	0.01	25.00	nA	
PFO Output Voltage		I _{SOURCE} =800 μ A	V _{CC} -1.5			V	
		I _{SINK} =3.2mA			0.4		

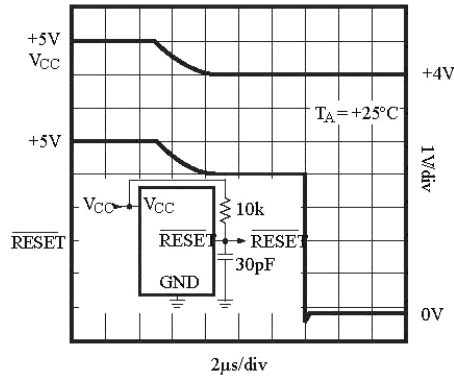
Note 2: Applies to both RESET in the MAX705-MAX708 and RESET in the MAX707/MAX708/MAX813L.

Typical Operating Characteristics

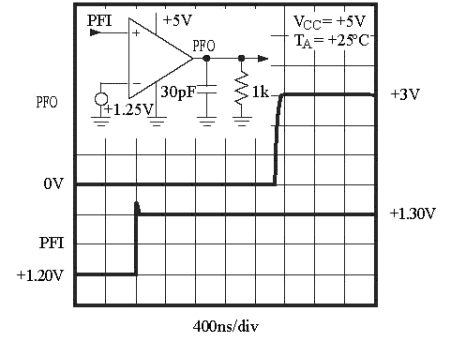
MAX705/MAX707
RESET OUTPUT VOLTAGE
vs. SUPPLY VOLTAGE



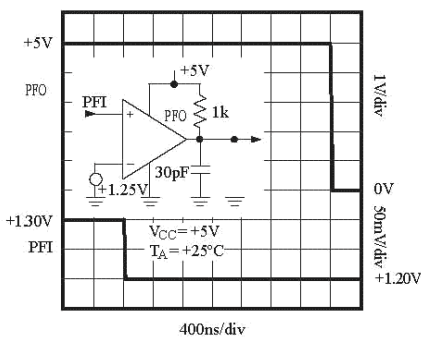
MAX705/MAX707
RESET RESPONSE TIME



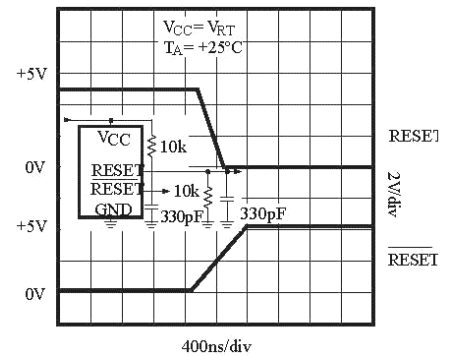
POWER-FAIL COMPARATOR
DE-ASSERTION RESPONSE TIME



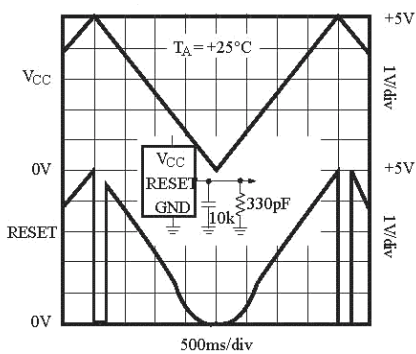
POWER-FAIL COMPARATOR
ASSERTION RESPONSE TIME



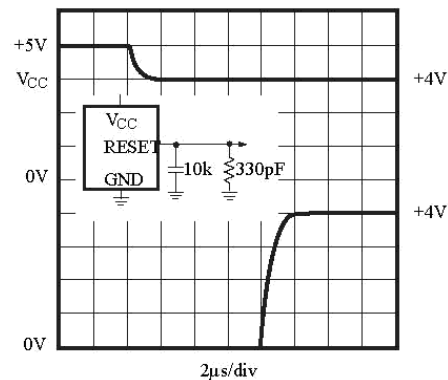
MAX707
RESET, RESET DE-ASSERTION



MAX707/MAX708/MAX813L
RESET OUTPUT VOLTAGE
Vs. SUPPLY VOLTAGE



MAX813L
RESET RESPONSE TIME



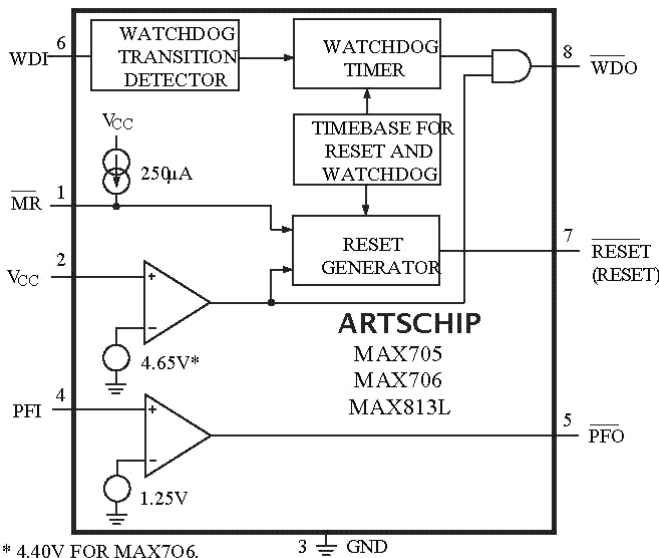


MAX705-MAX813L

Low-Cost, μ P Supervisory Circuit

Pin Description

PIN						NAME	FUNCTION
MAX705/MAX706		MAX707/MAX708		MAX813L			
DIP/SO	μ MAX	DIP/SO	μ MAX	DIP/SO	μ MAX		
1	3	1	3	1	3	MR	Manual-Reset Input triggers a reset pulse when pulled below 0.8V. This active-low input has an internal 250 μ A pull-up current. It can be driven from a TTL or CMOS logic line as well as shorted to ground with a switch.
2	4	2	4	2	4	Vcc	+5V Supply Input
3	5	3	5	3	5	GND	0V Ground Reference for all signals
4	6	4	6	4	6	PFI	Power-Fail Voltage Monitor Input. When PFI is less than 1.25V, PFO goes low. Connect PFI to GND or Vcc when not used.
5	7	5	7	5	7	PFO	Power-Fail Output goes low and sinks current when PFI is less than 1.25V; otherwise PFO stays high.
6	8	-	-	6	8	WDI	Watchdog Input. If WDI remains high or low for 1.6sec, the internal watchdog timer runs out and WDO goes low (Figure 1). Floating WDI or connecting WDI to a high-impedance three-state buffer disables the watchdog feature. The internal watchdog timer clears whenever reset is asserted, WDI is three stated, or WDI sees a rising or falling edge.
-	-	6	-	-	-	N.C.	No Connect
7	1	7	1	-	-	RESET	Active-Low Reset Output pulses low for 200ms when triggered, and stays low whenever Vcc is below the reset threshold (4.65V in the MAX705 and 4.40 V in the MAX706). It remains low for 200ms after Vcc rises above the reset threshold or MR goes from low to high (Figure 3). A watchdog timeout will not trigger RESET unless WDO is connected to MR.
8	2	-	-	8	2	WDO	Watchdog Output pulls low when the internal watchdog timer finishes its 1.6sec count and does not go high again until the watchdog is cleared. WDO also goes low during low-line conditions. Whenever Vcc is below the reset threshold, WDO stays low; however, unlike RESET, WDO does not have a minimum pulse width. As soon as Vcc rise above the reset threshold, WDO goes high with no delay.
-	-	8	2	7	1	RESET	Active-High Reset Output is the inverse of RESET. Whenever RESET is high, RESET is low, and vice versa (Figure 2). The MAX813L has a RESET output only.



* 4.40V FOR MAX706.
() ARE FOR MAX813L ONLY.

Figure 1. MAX705/MAX706/MAX813L Block Diagram

Detailed Description

Reset Output

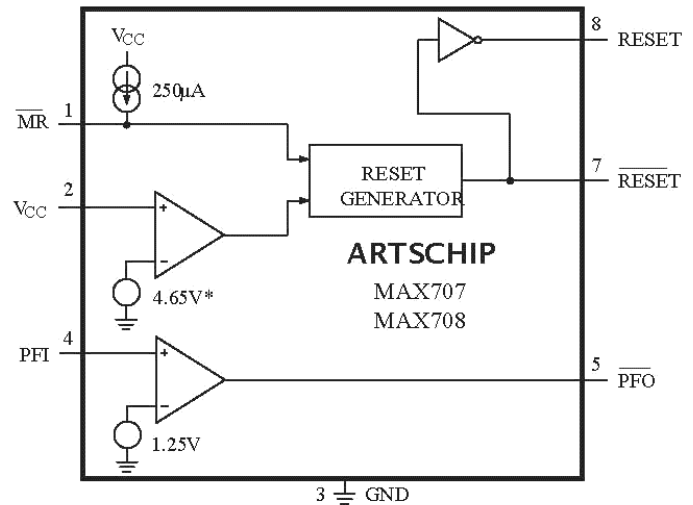
A microprocessor's (μ P's) reset input starts the μ P in a known state, whenever the μ P is in an unknown state. it should be held in reset. The MAX705-MAX708/MAX813L assert reset during power-up and prevent code execution errors during power-down or brownout conditions.

On power-up, once Vcc reaches 1V, RESET is a guaranteed logic low of 0.4V or less. As Vcc rises, RESET stays low. When Vcc rises above the reset threshold, an internal timer releases RESET after about 200ms. RESET pulses low whenever Vcc dips below the reset threshold, i.e. brownout condition. If brownout occurs in the middle of a previously initiated reset pulse, the pulse continues for at least another 140ms. On power-down, Once Vcc falls below the reset threshold, RESET stays low and is guaranteed to be 0.4V or less until Vcc drops below 1V.

The MAX707/MAX708/MAX813L active-high RESET output is simply the complement of the RESET output, and is guaranteed to be valid with Vcc down to 1.1V. Some μ Ps, such as Intel's 80C51, require an active-high reset pulse.

Watchdog Timer

The MAX705/MAX706/MAX813L watchdog circuit monitors the μ P's activity. If the μ P does not toggle the watchdog input (WDI) within 1.6sec and WDI is not three-stated, WDO goes low. As long as RESET is asserted or the WDI input is three-stated, the watchdog time will stay cleared and will not



* 4.40V FOR MAX706.

Figure 2. MAX707/MAX708 Block Diagram

count. As soon as reset is released and WDI is driven high or low, the timer will start counting. Pulse as short as 50ns can be detected.

Typically, WDO will be connected to the non-maskable interrupt input (NMI) of a μ P. When Vcc drops below the reset threshold, WDO will go low whether or not the watchdog timer has timed out yet. Normally this would trigger an NMI interrupt, but RESET goes low simultaneously, and thus overrides the NMI interrupt.

If WDI is left unconnected, WDO can be used as a low line output. Since floating WDI disables the internal timer, WDO goes low only when Vcc falls below the reset threshold, thus functioning as a low-line output.

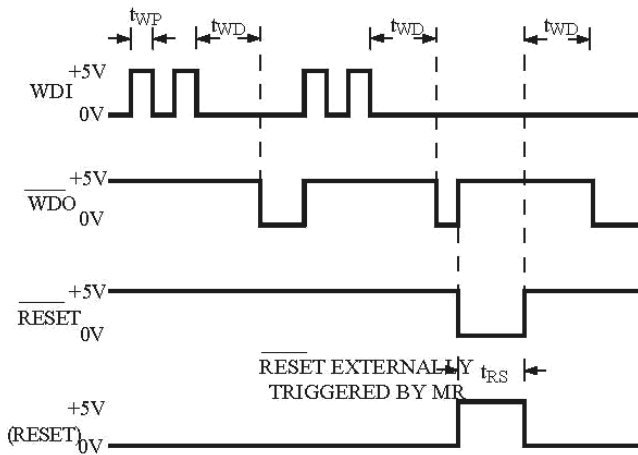
The MAX705/MAX706 have a watchdog timer and a RESET output. The MAX707/MAX708 have both active high and active-low reset outputs. The MAX813L has both an active-high reset output and a watchdog timer.

Manual Reset

The manual-reset input (MR) allows reset to be triggered by a pushbutton switch. The switch is effectively debounced by the 140ms minimum reset pulse width. MR is TTL/CMOS logic compatible, so it can be driven by an external logic line. MR can be used to force a watchdog timeout to generate a reset pulse in the MAX705/MAX706/MAX813L. Simply connect WDO to MR.

Power-Fail Comparator

The power-fail comparator can be used for various purposes because its output and noninverting input are not internally connected. The inverting input is internally connected to a 1.25V reference.



() ARE FOR MAX813L ONLY.

Figure 3. MAX705/MAX706/MAX813L Watchdog Timing.

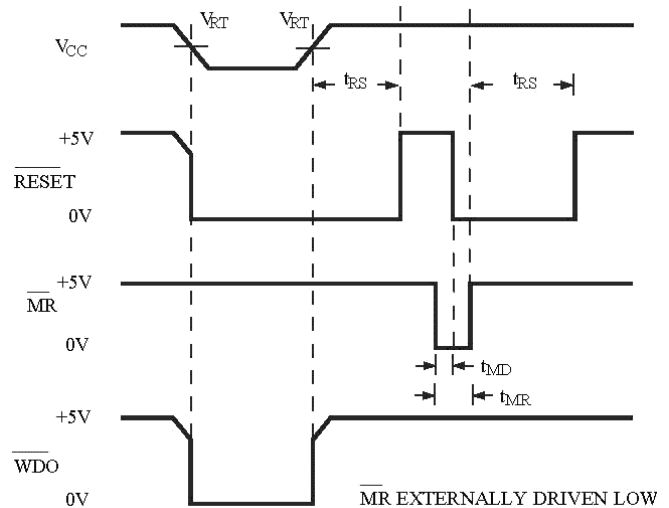


Figure 4. MAX705/MAX706 RESET, MR, and WDO Timing with WDI Three-Stated. The MAX707/MAX708/MAX813L RESET output is the inverse of RESET shown.

To build an early-warning circuit for power failure, connect the PFI pin to a voltage divider (see Typical Operating Circuit). Choose the voltage divider ratio so that the voltage at PFI falls below 1.25V just before the +5V regulator drops out. Use PFO to interrupt the μ P so it can prepare for an orderly power-down.

Applications Information

Ensuring a Valid RESET

Output Down to $V_{CC}=0V$ When V_{CC} falls below 1V, the MAX705-MAX708 RESET output no longer sinks current – it becomes an open circuit. High-impedance CMOS logic inputs can drift to undetermined voltages if left undriven. If a pull-down resistor is added to the RESET pin as shown in Figure 5, any stray charge or leakage currents will be drained to ground, holding RESET low. Resistor value (R_1) is not critical. It should be about 100K Ω , large enough not to load RESET and small enough to pull RESET to ground.

Monitoring Voltages Other Than the Unregulated DC Input

Monitor voltages other than the unregulated DC by connecting a voltage divider to PFI and adjusting the ratio appropriately. If required, add hysteresis by connecting a resistor (with a value approximately 10 times the sum of the two resistors in the potential divider network) between PFI and PFO. A capacitor between PFI and GND will reduce the power-fail circuit's

sensitivity to high-frequency noise on the line being monitored. RESET can be asserted on other voltages in addition to the +5V V_{CC} line. Connect PFO to MR to initiate a RESET pulse when PFI drops below 1.25V. Figure 6 shows the MAX705-MAX708S configured to assert RESET when the +5V supply falls below the reset threshold, or when the +12V supply falls below approximately 11V.

Monitoring a Negative Voltage

The power-fail comparator can also monitor a negative supply rail (Figure 7). When the negative rail is good (a negative voltage of large magnitude), PFO is low, and when the negative rail is degraded (a negative voltage of lesser magnitude), PFO is high. By adding the resistors and transistor as shown, a high PFO triggers reset. As long as PFO remains high, the MAX705-MAX708/MAX813L will keep reset asserted (RESET=low, RESET =high). Note that this circuit's accuracy depends on the PFI threshold tolerance, the V_{CC} line, and the resistors.

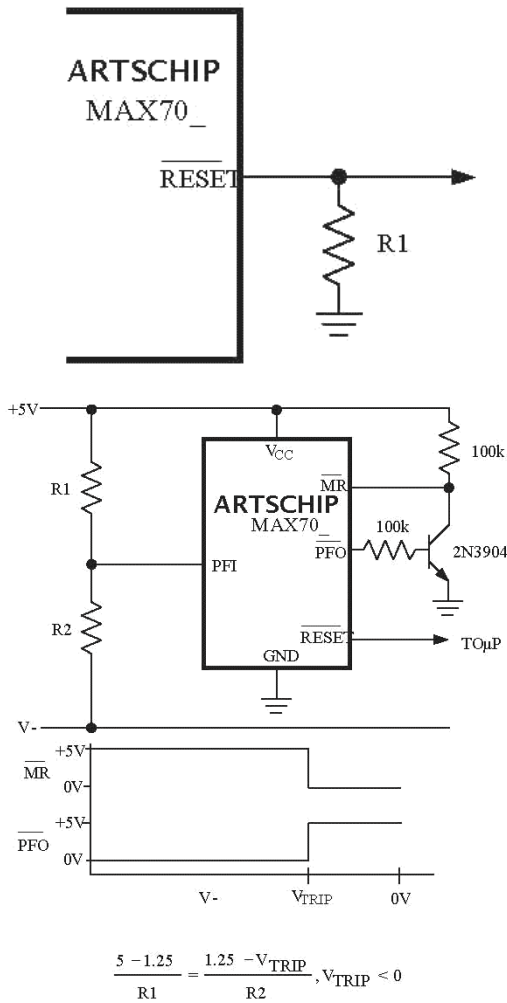
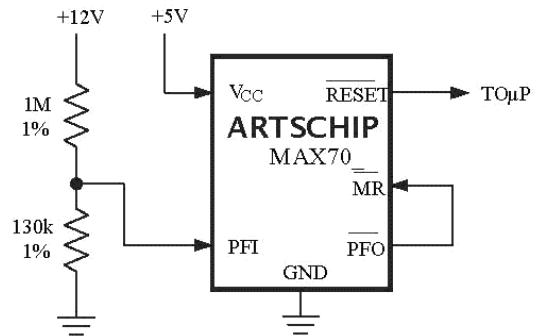


Figure 7. Monitoring a Negative Voltage



PARAMETER	MIN	TYP	MAX	UNIT
+12V Reset Threshold at +25 °C	10.67	10.87	11.50	V

Figure 6. Monitoring Both +5V and +12V

BUFFERED RESET TO OTHER SYSTEM COMPONENTS

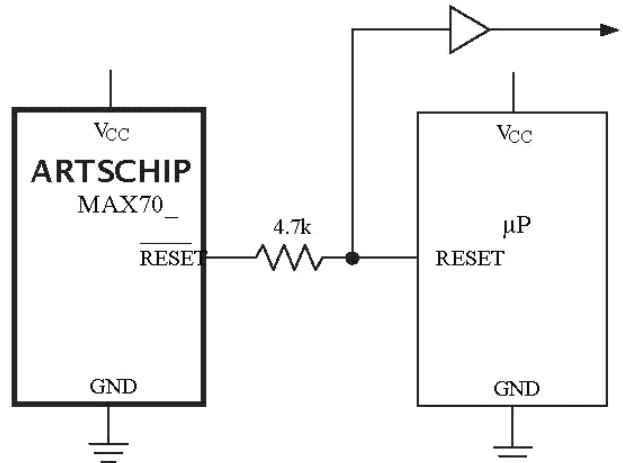


Figure 8. Interfacing to μ Ps with Bidirectional Reset I/O

Interfacing to μ Ps with Bidirectional Reset Pins

μ Ps with bidirectional reset pins, such as the Motorola 68HC11 series, can contend with the MAX705-MAX708 RESET output. If, for example, the RESET output is driven high and the μ P wants to pull it low, indeterminate logic levels may result. To correct this, connect a 4.7k Ω resistor between the RESET output and the μ P reset I/O, as in Figure 8. Buffer the RESET output to other system components.

Ordering Information (continued)

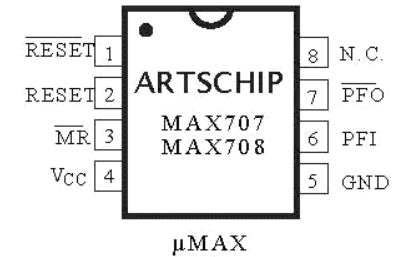
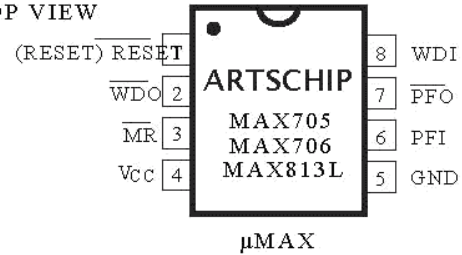
PART	TEMP. RANGE	PIN-PACKAGE
MAX705EPA	-40 to +85	8 Plastic DIP
MAX705ESA	-40 to +85	8 SO
MAX705EUA	-40 to +85	8 μ MAX
MAX705MJA	-55 to +125	8 CERDIP**
MAX706CPA	0 to +70	8 Plastic DIP
MAX706CSA	0 to +70	8 SO
MAX706CUA	0 to +70	8 μ MAX
MAX706C/D	0 to +70	Dice *
MAX706EPA	-40 to +85	8 Plastic DIP
MAX706ESA	-40 to +85	8 SO
MAX706EUA	-40 to +85	8 μ MAX
MAX706MJA	-55 to +125	8 CERDIP**
MAX707CPA	0 to +70	8 Plastic DIP
MAX707CSA	0 to +70	8 SO
MAX707CUA	0 to +70	8 μ MAX
MAX707C/D	0 to +70	Dice *
MAX707EPA	-40 to +85	8 Plastic DIP
MAX707ESA	-40 to +85	8 SO
MAX707EUA	-40 to +85	8 μ MAX
MAX707MJA	-55 to +125	8 CERDIP**
MAX708CPA	0 to +70	8 Plastic DIP
MAX708CSA	0 to +70	8 SO
MAX708CUA	0 to +70	8 μ MAX
MAX708C/D	0 to +70	Dice*
MAX708EPA	-40 to +85	8 Plastic DIP
MAX708ESA	-40 to +85	8 SO
MAX708EUA	-40 to +85	8 μ MAX
MAX708MJA	-55 to +125	8 CERDIP**
MAX813LCPA	0 to +70	8 Plastic DIP
MAX813LCSA	0 to +70	8 SO
MAX813LCUA	0 to +70	8 μ MAX
MAX813LC/D	0 to +70	Dice*
MAX813LEPA	-40 to +85	8 Plastic DIP
MAX813LESA	-40 to +85	8 SO
MAX813LMUA	-40 to +85	8 μ MAX
MAX813LMJA	-55 to +125	8 CERDIP**

*Dice are specified at TA=+25 .

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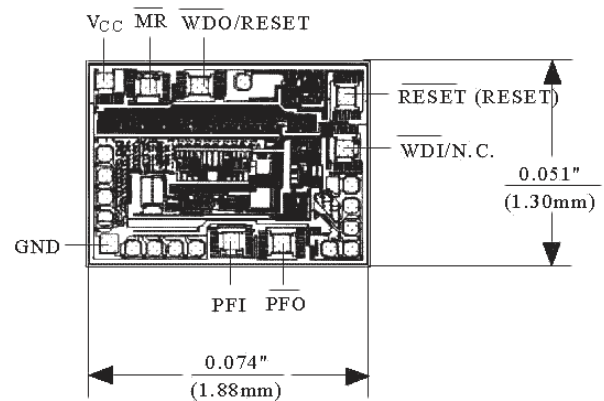
Pin Configuration (continued)

TOP VIEW



() ARE FOR MAX813L ONLY.

Chip Topography



() ARE FOR MAX813L ONLY.

TRANSISTOR COUNT: 572

SUBSTRATE MUST BE LEFT UNCONNECTED.

Package Information

